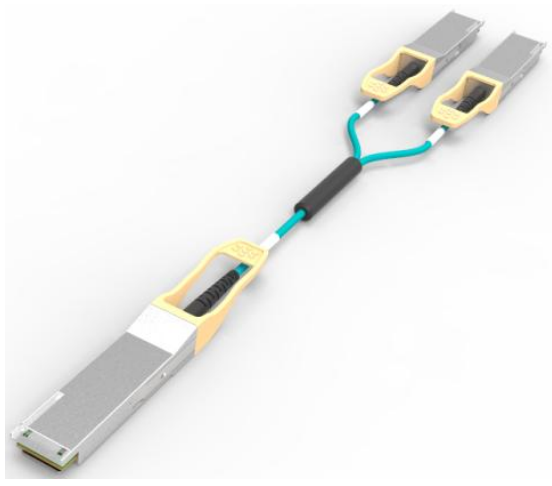
400G QSFP112 to 2 x 200G QSFP56 AOC Optical Transceiver Module

FYJH-400MxxxC

Features

- ✓ Hot-plug QSFP112 and QSFP56 form factor
- ✓ 4x106.25Gbps PAM4 transmitter and PAM4 receiver (The QSFP112 End)
- ✓ 4 channels 850nm VCSEL array and PIN photo detector array (The QSFP112 End)
- ✓ Power consumption <8W(The QSFP112 End)
- ✓ 2 channels 850nm VCSEL array and PIN photo detector array (The QSFP56 End)
- ✓ Power consumption <5W(The QSFP56 End)
- ✓ 4x53.125Gbit/s PAM4 electrical interface(200GAUI-4) (The QSFP56 End)
- ✓ 2x106.25Gbps PAM4 Optics architecture(The QSFP56 End)
- ✓ Compliant to QSFP112&QSFP56 MSA and CMIS
- ✓ Maximum link length of 30m on OM3 Multimode Fiber (MMF)and 50m on OM4 MMF with FEC
- ✓ Built-in digital diagnostic functions
- ✓ Operating case temperature 10°C to +70°C
- ✓ 3.3V power supply voltage
- ✓ RoHS compliant(lead free)

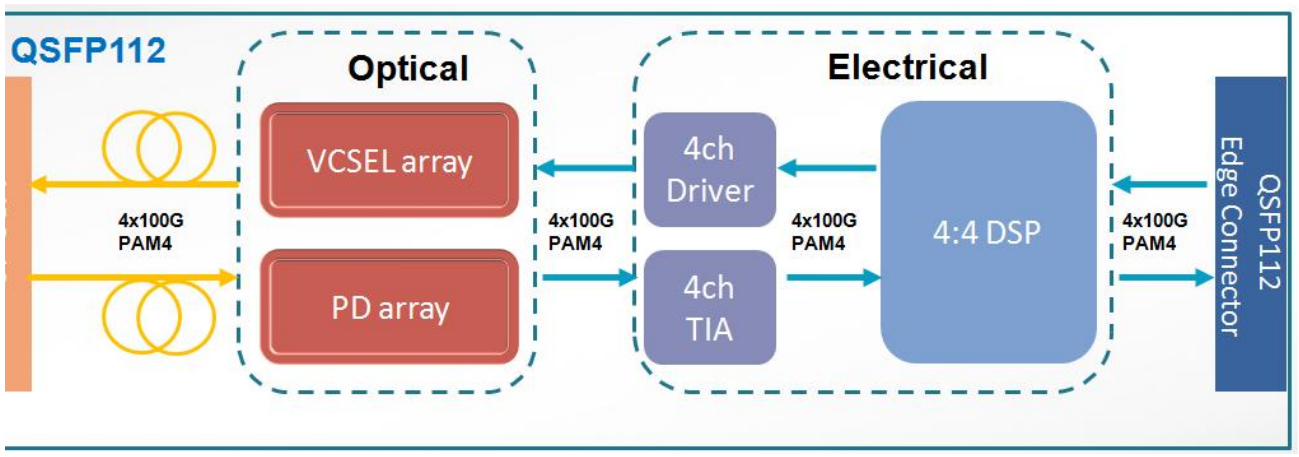


Applications

- ✓ IEEE 802.3db 400GBASE-VR4 Ethernet (PAM4)
- ✓ The transceiver is designed for Ethernet, Telecom and Infiniband use cases.

Description

FIBERSTAMP's FYJH-400MxxxC MMF Active Optical Cable is used in 4 X 100Gigabit Ethernet links over OM3/OM4 multimode fiber. The QSFP112 port has integrate 4 independent transmit and receive channels, each capable of 106.25Gb/s PAM4 operation for an aggregate data rate of 425Gb/s. The QSFP56 module can convert 4-channel 53.125Gb/s electrical data to 2 parallel channels of optical signals, each supporting106.25Gb/s data transmission. Reversely, it can convert 2-channel 106.25Gb/s optical signals to 4-channel electrical output data on the receiver side. It is compliant with IEEE 802.3db, and QSFP112&QSFP56 MSA.



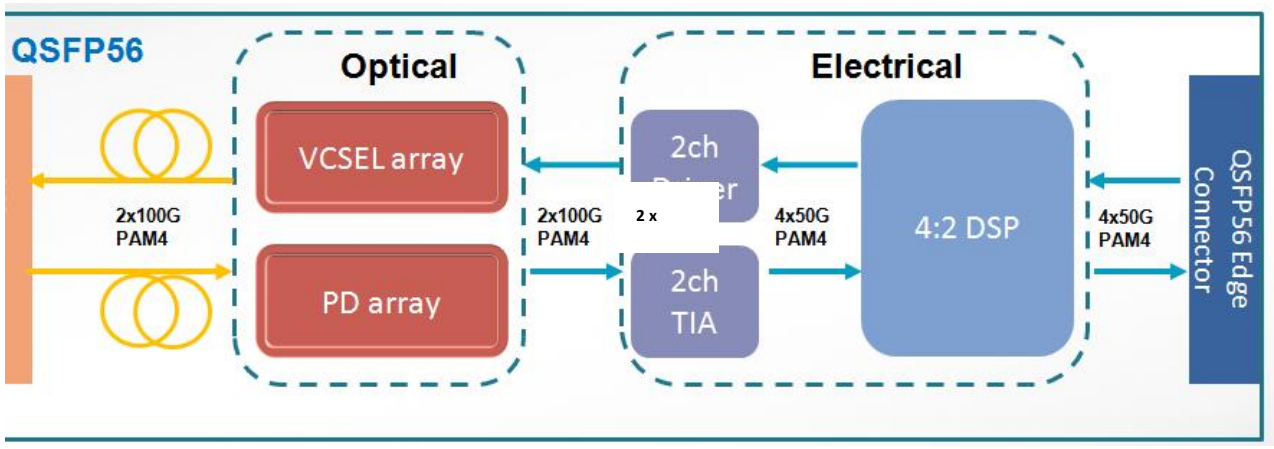


Figure1. Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-20	85	°C
Case Operating	Top	10	70	°C
Humidity(non-condensing)	Rh	5	85	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tca	10		70	°C
Data Rate Per Lane			106.25		Gbps
Humidity	Rh	5		85	%
Power Dissipation(The QSFP112 End)	Pm		7.5	8	W
Power Dissipation(The QSFP56 End)	Pm		4.5	5	W

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential Output impedance	Zout	90	100	110	ohm
Differential input voltage	ΔVin	400		900	mVp-p
Differential output voltage	ΔVout			850	mVp-p
Bit Error Rate	BER			2.4E-4	-
Input Logic Level High	V_{IH}	2.0		V_{cc}	V
Input Logic Level Low	V_{IL}	0		0.8	V
Output Logic Level High	V_{OH}	V_{cc}-0.5		V_{cc}	V
Output Logic Level Low	V_{OL}	0		0.4	V
Input Logic Level High	V_{IH}	2.0		V_{cc}	V

Note:

1. BER=2.4E-4; Pre-FEC.
2. Differential input voltage amplitude is measured between TxnP and TxnN.
3. Differential output voltage amplitude is measured between RxnP and RxnN.

Optical Characteristics

Table 3 - Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Centre Wavelength	λc	842	850	948	nm	_
RMS spectral width	Δλ	-	-	0.65	nm	_
Average launch power, each lane	Pout	-4.6	-	5.5	dBm	-
Optical Modulation Amplitude (OMAouter), each lane	OMA	-2.6		4	dBm	-
Transmitter and dispersion eye closure for PAM4(TDECQ),each	TDECQ			4.4	dB	
Extinction Ratio	ER	2.5	-	-	dB	-
Average launch power of OFF transmitter, each lane				-30	dB	-
Receiver						
Centre Wavelength	λc	842	850	948	nm	-
Receiver Sensitivity in OMAout	RXsen			max (-4.4,TECQ-6.2)	dBm	1
Stressed Receiver Sensitivity in OMAout	SRS			-1.8	dBm	2
Maximum Average power at receiver , each lane				5.5	dBm	-
Minimum Average power at receiver , each		-6.3			dBm	
Receiver Reflectance				-15	dB	-
LOS Assert	LOSA	-15		-8.5	dBm	-
LOS De-Assert	LOSD			-6.5	dBm	-
LOS Hysteresis	LOSH	0.5			dB	-

Note：

1. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC.
2. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Digital Diagnostic Specification

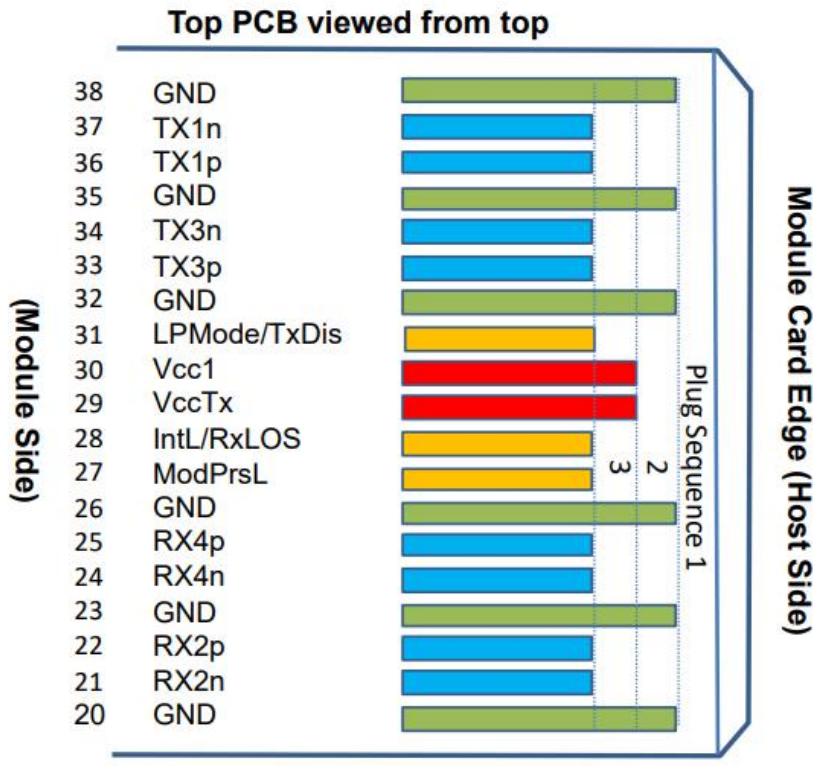
Parameter	Symbol	Min	Typical	Max	Units	Notes
Transceiver Case Temperature	DMI_Temp	-3		+3	℃	Over operating temp
Supply voltage monitor absolute error	DMI _VCC	-0.1		0.1	V	Full operating range
Channel RX power monitor absolute error	DMI_RX	-2		+2	dB	Per channel
Channel Bias current monitor	DMI_Ibias	-10%		+10%	mA	Per channel
Channel TX power monitor absolute error	DMI_TX	-2		+2	dB	Per channel

Pin Description

Electrical Pin Definition

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	TWI serial interface clock	3	
12	LVCMOS-I/O	SDA	TWI serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/ RxLOS	Interrupt/optional RxLOS	3	
29		VccTx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode/ TxDis	Low Power mode/optional TX Disable	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Note 1: QSFP112 uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector Gnd contact is rated for a maximum current of 500 mA.
Note 2: VccRx, Vcc1, and VccTx shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector are listed in Table 13. For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a maximum current of 1500 mA.
Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1, 2, and 3 see Figure 14 for pad locations.



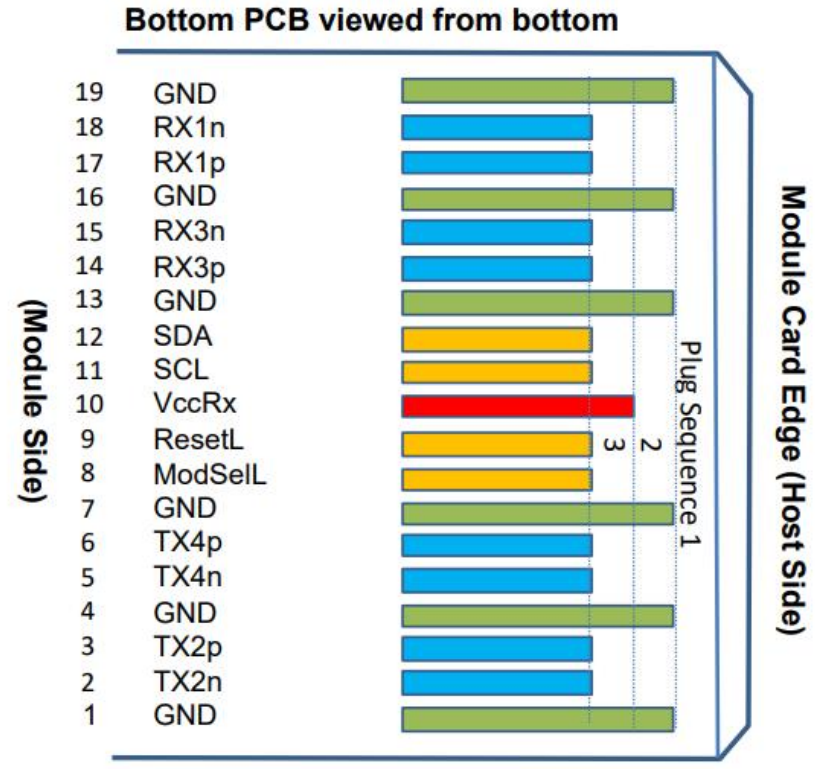


Figure2. Electrical Pin-out Details

ModSelL Pin

The ModSelL is an input signal that shall be pulled to Vcc in the QSFP112 modules. When held low by the host, the module responds to TWI serial communication commands. The ModSelL allows the use of multiple QSFP112 modules on a single TWI interface bus. When ModSelL is "High", the module shall not respond to or acknowledge any TWI interface communication from the host.

In order to avoid conflicts, the host system shall not attempt TWI interface communications within the ModSelL de-assert time after any QSFP112modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL Pin

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state.

LPMode/TxDis Pin

LPMode/TxDis is a dual-mode input signal from the host operating with active high logic. It shall be pulled towards Vcc in the module. At power-up or after ResetL is deasserted LPMode/TxDis behaves as LPMode. If supported, LPMode/TxDis can be configured as TxDis using the TWI interface except during the execution of a reset.

ModPrsL Pin

ModPrsL shall be pulled up to Vcc Host on the host board and pulled low in the module. The ModPrsL is asserted

"Low" when the module is inserted. The ModPrsL is deasserted "High" when the module is physically absent from the host connector due to the pull-up resistor on the host board.

IntL/RxLOSL Pin

IntL/RxLOSL is a dual-mode active-low, open-collector output signal from the module. It shall be pulled up towards Vcc on the host board. At power-up or after ResetL is released to high, IntL/RxLOSL is configured as IntL. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the TWI serial interface. The IntL signal is deasserted "High" after all set interrupt flags are read. If dual mode operation supported, IntL/RxLOSL can be optionally programmed as RxLOSL using the TWI interface except during the execution of a reset. If the module has no interrupt flags asserted (IntL/RxLOSL is high), there should be no change in IntL/RxLOSL states after the mode change.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure3.

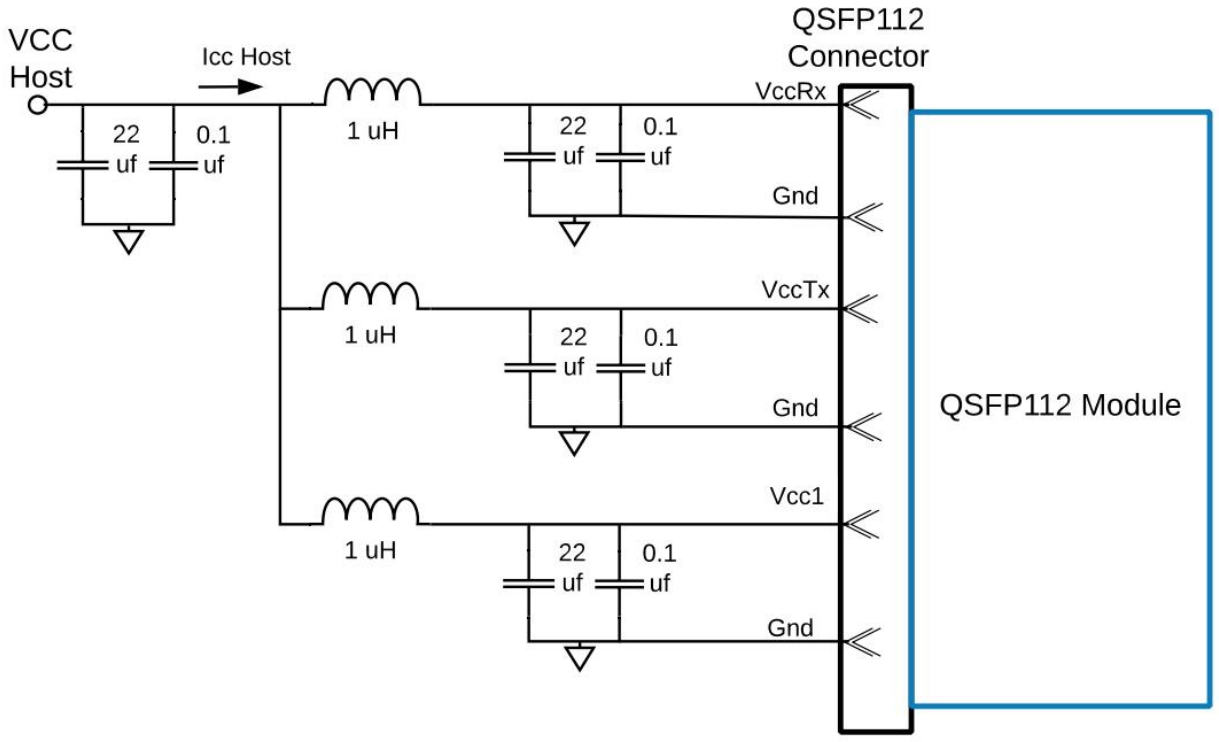


Figure3. Host Board Power Supply Filtering

DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics monitoring function is available on all FIBERSTAMP products. A 2-wire serial interface provides user to contact with module.

Memory Structure and Mapping

This limits the management memory that can be directly accessed by the host to 256 bytes, which is divided in Lower Memory (addresses 00h through 7Fh) and Upper Memory (addresses 80h through FFh).

A larger addressable management memory is required for all but the most basic modules. This is supported by a structure of 128-byte pages, together with a mechanism for dynamically mapping any of the 128-byte pages from a larger internal management memory space into Upper Memory the host addressable space.

The addressing structure of the additional internal management memory is shown in Figure 4 The management memory inside the module is arranged as a unique and always host accessible address space of 128 bytes (Lower Memory) and as multiple upper address subspaces of 128 bytes each (Pages), only one of which is selected as host visible in Upper Memory. A second level of Page selection is possible for Pages for which several instances exist (e.g. where a bank of pages with the same Page number exists).

This structure supports a flat 256 byte memory for passive copper modules and permits timely access to addresses in the Lower Memory, e.g. Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function in the Lower Page. For more complex modules which require a larger amount of management memory the host needs to use dynamic mapping of the various Pages into the host addressable Upper Memory address space, whenever needed.

Note: The management memory map has been designed largely after the QSFP memory map. This memory map has been changed in order to accommodate 8 electrical lanes and to limit the required memory space. The single

address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

Supported Pages

A basic 256 byte subset of the Management Memory Map is mandatory for all CMIS compliant devices. Other parts are only available for paged memory modules, or when advertised by the module. See CMIS V4.0 for details regarding the advertisement of supported management memory spaces.

In particular, support of the Lower Memory and of Page 00h is required for all modules, including passive copper cables. These pages are therefore always implemented. Additional support for Pages 01h, 02h and bank 0 of Pages 10h and 11h is required for all paged memory modules.

Bank 0 of pages 10h-1Fh, provides lane-specific registers for the first 8 lanes, and each additional bank provides support for additional 8 lanes. Note, however, that the allocation of information over the banks may be page specific and may not to be related to grouping data for 8 lanes.

The structure allows address space expansion for certain types of modules by allocating additional Pages. Moreover, additional banks of pages.

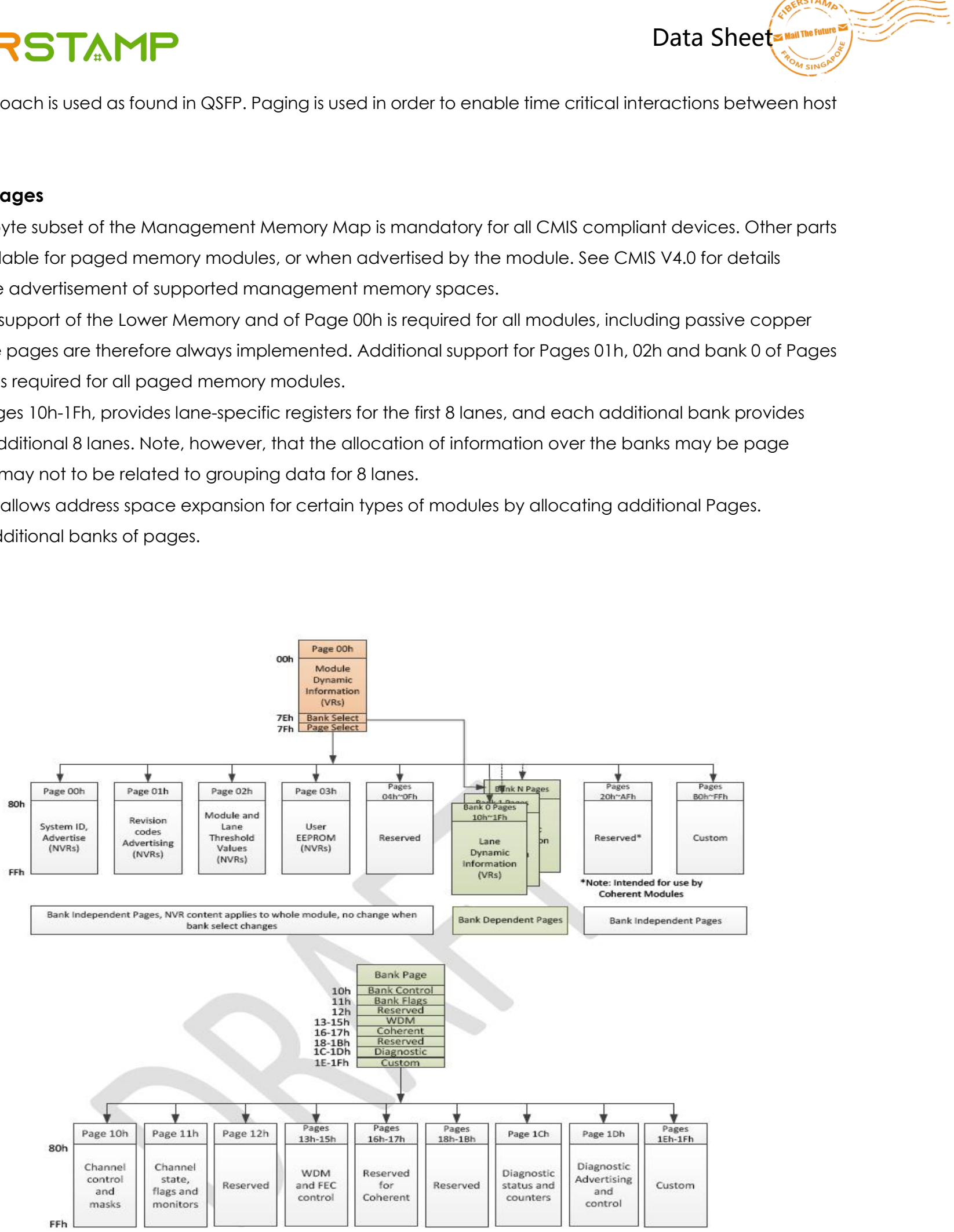


Figure4. Memory Map

Mechanical Dimensions(mm)

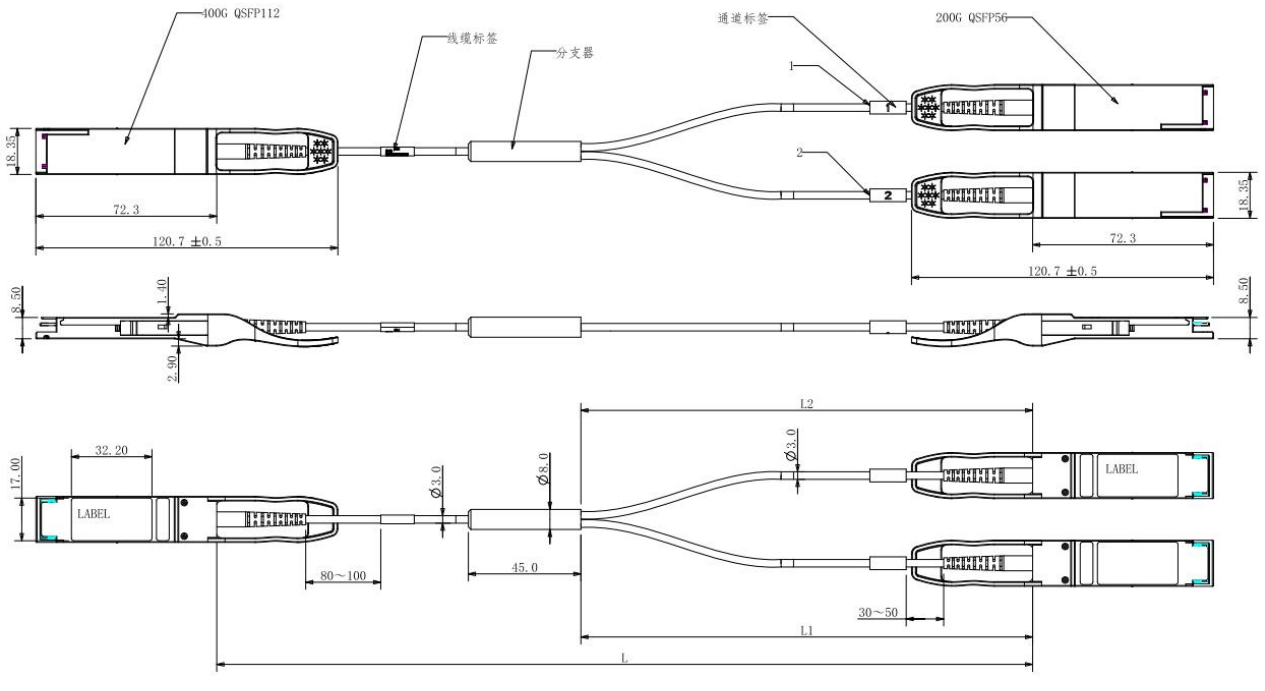


Figure5. Mechanical Specifications

Regulatory Compliance

FIBERSTAMP FYJH-400MxxxC transceivers are Class 1 Laser Products. They are certified per the following standards:

Feature	Standard
Laser Safety	IEC 60825-1:2014 (3rd Edition) IEC 60825-2:2004/AMD2:2010 EN 60825-1-2014 EN 60825-2:2004+A1+A2
Electrical Safety	EN 62368-1: 2014 IEC 62368-1:2014 UL 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032：2015 EN55035：2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B ANSI C63.4-2014

References

1. QSFP112 MSA&QSFP56 MSA
2. CMIS V4.0/V5.2
3. IEEE 802.3db400GBASE-VR4 Ethernet (PAM4)
4. IEEE802.3ck

⚠CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering information

Part Number	Product Description
FYJH-400MxxxC	400G QSFP112 - 2x200G QSFP56 AOC transceiver, 850nm, up to 50m with OM4, XXX: 001-1m, 005-5m, 007-7m, 020-20m, 030-30m, 050-50m

Important Notice

Performance figures, data and any illustrative material provided in this data sheet are typical and must be

specifically confirmed in writing by FIBERSTAMP before they become applicable to any particular order or contract. In accordance with the FIBERSTAMP policy of continuous improvement specifications may change without notice. The publication of information in this data sheet does not imply freedom from patent or other protective rights of FIBERSTAMP or others. Further details are available from any FIBERSTAMP sales representative.

E-mail: sales@fiberstamp.com
Official Site: www.fiberstamp.com

Revision History

Revision	Date	Description
V0	Dec-29-2025	Advance Release.